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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,235	06/29/2001	Martin Hurich	10191/1839	9413

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EXAMINER	
PORTKA, GARY J	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/896,235	HURICH, MARTIN	
	Examiner	Art Unit	
	Gary J Portka	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 16, 2004 has been entered.

2. Claims 1 and 4 were amended by Applicant. Claims 1-4 are pending.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Fleming et al., U.S. Patent 6,412,080 B1.

5. As to claims 1 and 4, Fleming discloses the *method and controller for writing/erasing a non-volatile memory* (Fig. 1, 22, and Fig. 2), *writing a release pattern into first subareas after error-free writing* (Fig. 2, FlashRecordHeader 36 Invalid bit cleared, see col. 5 lines 16-34, in particular second and third entries of table), and

writing an invalidity pattern prior to an erase (FlashRecordHeader 36 notDeleted bit cleared, see col. 5 lines 16-34, in particular fourth entry of table); *the second subareas include an initial and last subarea* (see Fig. 2, since there are a plurality of FlashRecordHeaders, each with notDeleted bits, the one nearest the top of the sector is seen as the initial subarea, and the one nearest the bottom of the sector is seen as the last subarea of the second subareas).

6. As to claim 2, in Fleming the patterns (bits) do not correspond to the contents of erased modules, but rather to data records, a plurality of which compose an erasable module (sector).

7. As to claim 3, in Fleming the second subareas (notDeleted bits) are checked for presence prior to reading out a written area (since if they are cleared the record is ignored).

8. Claim 4 is rejected under 35 U.S.C. 102(e) as being anticipated by Nagase et al., U.S. Patent 6,154,808.

9. As to claim 4, Nagase discloses *a controller comprising a storage device having non-volatile memory area* (see Title, Abstract, Fig. 2)) for *storing control function programs and control function data* (statement of intended use, and non-functional descriptive language), *including at least one first subarea for release patterns which occupy subareas in the written memory area* (even numbered bit locations, Figs. 4(a)-(h)), *and the memory area further including second subareas for invalidity patterns, the second subareas including an initial and a last subarea of the memory area* (odd numbered bit locations; see col. 3 line 16 to col. 4 line 14, where it is described that e.g.

when as shown in Figs. 4(a) and (b), when the first bit is cleared, the sector is considered invalid, as shown in Figs. 4(b) and (c), when the second bit is cleared, the sector is considered valid = released, etc., the first odd bit and the last odd bit seen as the recited initial and last subareas; or alternatively as seen in Figs. 2-3, the initial subarea seen as the odd bits of the first flag area 12, and the last subarea the odd bits of the last flag area 12).

10. Claim 4 is rejected under 35 U.S.C. 102(e) as being anticipated by Haroun et al., U.S. Patent 6,532,514 B1.

11. As to claim 4, Haroun discloses *a controller comprising a storage device having non-volatile memory area* (see Title, Abstract, Fig. 1)) for *storing control function programs and control function data* (statement of intended use, and non-functional descriptive language), *including at least one first subarea for release patterns which occupy subareas in the written memory area* (the second active indicators, see col. 4 lines 27-33), *and the memory area further including second subareas for invalidity patterns, the second subareas including an initial and a last subarea of the memory area* (first active indicators, see col. 4 lines 19-22; also see col. 3 lines 56-67, col. 4 lines 8-10, and table in col. 4, which show that programmed first active indicators indicate invalidity, while programmed second active indicators indicate validity; further, there are a plurality, and therefore initial and last subareas, of second active indicators).

Response to Arguments

12. Applicant's arguments filed December 16, 2004 have been fully considered but are largely moot in view of the new grounds of rejection. However, Examiner notes that

the statement on page 4 of that response, "that both the initial subarea and the last subarea of the memory area (relative to address) are second subareas" (emphasis added), is not supported by the disclosure. At page 6 the disclosure states "the first and last of the reserved subareas" (emphasis added) are the second subareas, and the Figure further apparently shows data at what would be the initial and last subareas of the memory area, not the invalidity pattern. Therefore, the claim language "an initial" and "a last subarea of the memory area" are interpreted above as simply initial and last subareas of the memory area that serve as the second subareas.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent No:

6,453,397 Flash storing earse, write, and read inhibition flags.

6,393,513 Flash storing old/new and used/free flags for each sector.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary J Portka
Primary Examiner
Art Unit 2188

February 17, 2004